MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

EEE4186 - VLSI SYSTEM DESIGN AND MODELING TECHNIQUE

(EE)

15 MARCH 2018
2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **5 pages** including cover page with **4 Questions** only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is the same.

3. Please print all your answers in the answer Booklet provided.

4. **A VHDL model** means an entity-architecture pair, plus any extra codes that might be necessary for them to work properly (library, use, etc.)

5. When names (of entities, architectures, signals, etc.) are not specified, you may use any suitable and valid name.

Question 1

(a) A multiplexer circuit diagram is shown in Figure Q1 which consists of an inverter, two AND gate and an OR gate.
(i) Construct the ***entity*** of this circuit using entity name: *mux2*.

[4 marks]

(ii) Write the ***architecture*** of this circuit using **structural** VHDL code by instantiate ***component*** *inv*, *and2* and *or2*. Use architecture name: *mux2_arch*.

[11 marks]

(iii) Construct the **complete** RTL VHDL code for a 2-to-1 multiplexer, using **Selected Signal Assignment**. Do not use logic gate assignment in the code.

[5 marks]

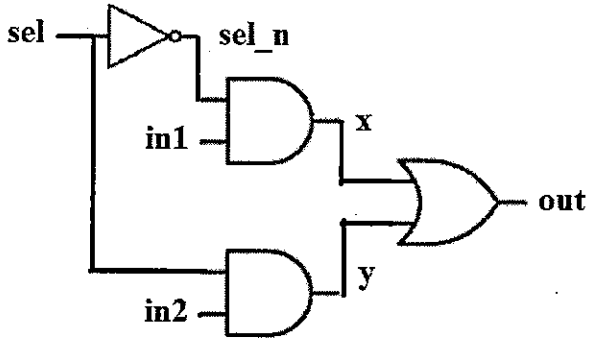

Figure Q1

(b) The simulation of a VHDL model operates in three phases. Describe and briefly elaborate each of these three phases.

[5 marks]

Continued ...

Question 2

(a) Using **standard logic gates**, write and construct the **complete** VHDL code (do not use structural VHDL code) for the circuit diagram shown in Figure Q2a.

[6 marks]

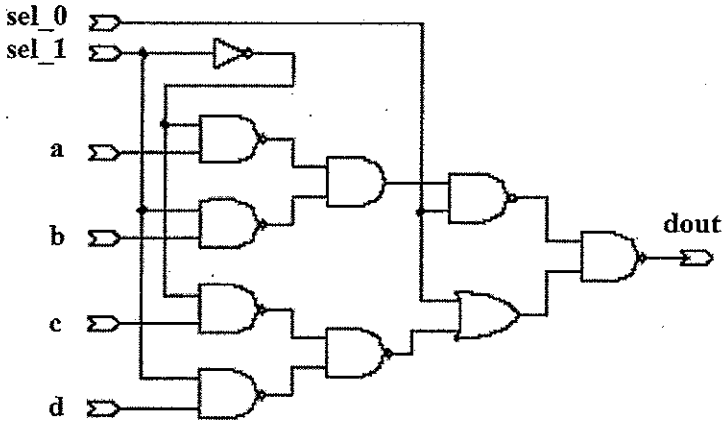

Figure Q2a

(b) Evaluate, compare and describe the differences between ***function*** and ***procedure*** in VHDL.

[6 marks]

(c) Write the **complete** synthesizable VHDL code for the logic diagram shown in Figure Q2b. The D-flip-flop is triggered by negative-edge clock C, with an asynchronous reset CLR signal.

[7 marks]

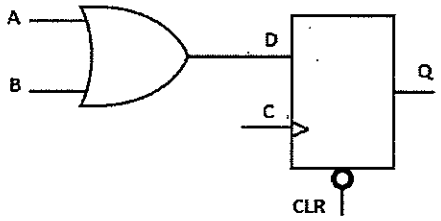

Figure Q2b

(d) Construct a simple fan speed controller using ***case*** statement in VHDL to represent the next speed of the fan (Output signal: *next_speed*). Define new *type* as low, medium and high. Create new *type* for this functional and write the ***process*** statement of VHDL code.

[6 marks]

Continued ...

Question 3

(a) Sketch the circuit diagram for the synthesizable VHDL code shown in Figure Q3 using 2-to-1 multiplexers.

[7 marks]

```
entity circuit is
port (b : in  std_logic_vector(3 downto 0);
      n : out std_logic_vector(2 downto 0));
end circuit;

architecture rtl of circuit is
begin
      n <=
            "100" when b(3)='1' else
            "011" when b(2)='1' else
            "010" when b(1)='1' else
            "001" when b(0)='1' else
            "000" ;
end rtl;
```

Figure Q3

(b) Re-write the entire synthesizable VHDL code shown in Figure Q3 using ***if-else*** statements.

[7 marks]

(c) Create a test-bench in VHDL code to test the circuit in part (a), by referring to the *work.circuit(beh)*. The time step for the test-bench is 100ns.

[8 marks]

(d) Sketch a waveform diagram to represent the test-bench signal(s) that you created in part (c), and include the expected output in your waveform.

[3 marks]

Continued ...

Question 4

(a) Create the VHDL code for the Mealy finite state machine (FSM) shown in Figure Q4. Use separate ***process*** statement for combinational and sequential logic. Note that **Reset** is asynchronous reset signal, **x** is the input signal and **out** is the output signal.

[18 marks]

signal orientation : x / out

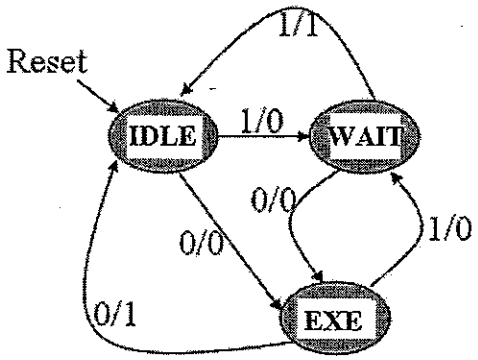

Figure Q4

(b) Sketch the function block diagrams for Moore and Mealy FSM, and write the output vector function for both FSM. Describe the difference between both in terms of output waveform.

[7 marks]

End of Paper